

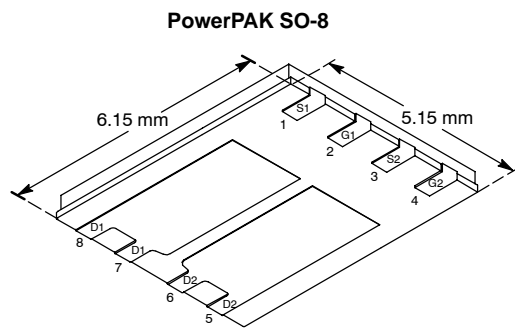


Dual P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
-60	0.064 @ $V_{GS} = -10$ V	-5	26
	0.080 @ $V_{GS} = -4.5$ V	-4.5	

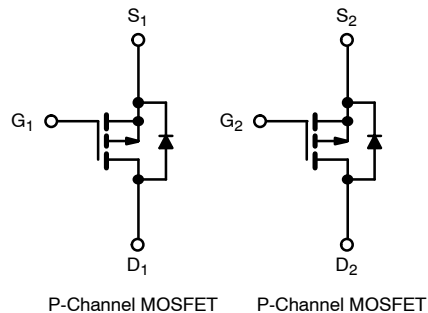
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile



Bottom View

Ordering Information: Si7949DP-T1—E3



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-60		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-5	-3.2	A
		$T_A = 70^\circ\text{C}$	-4	-2.6	
Pulsed Drain Current	I_{DM}	-25			
Continuous Source Current (Diode Conduction) ^a	I_S	-2.9	-1.2		
Avalanche Current	$L = 0.1$ mH	I_{AS}	22		
Single Pulse Avalanche Energy			E_{AS}	24.2	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.5	1.5	W
		$T_A = 70^\circ\text{C}$	2.2	0.94	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	27	36	$^\circ\text{C}/\text{W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	3.3	4.3		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

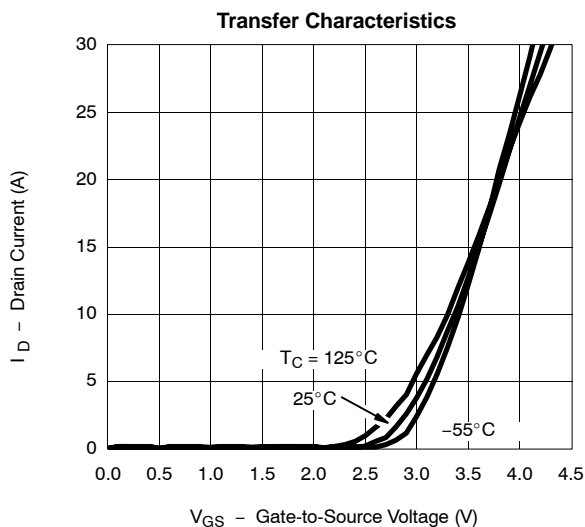
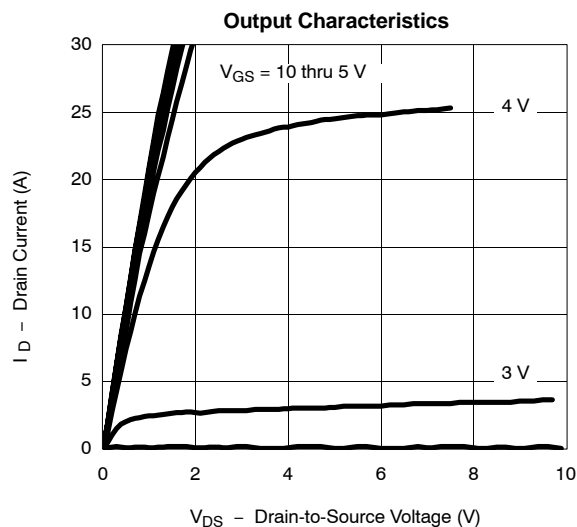
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1		-3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 70 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-25			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -5 A		0.051	0.064	Ω
		V _{GS} = -4.5 V, I _D = -4.5 A		0.064	0.080	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -5 A		16		S
Diode Forward Voltage ^a	V _{SD}	I _S = -2.9 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -5 A		26	40	nC
Gate-Source Charge	Q _{gs}		4.5			
Gate-Drain Charge	Q _{gd}		7.0			
Gate-Resistance	R _g			7.0		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, R _L = 30 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 6 Ω		8	15	ns
Rise Time	t _r		9	15		
Turn-Off Delay Time	t _{d(off)}		65	100		
Fall Time	t _f		30	45		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -5 A, di/dt = 100 A/μs		41	70	

Notes

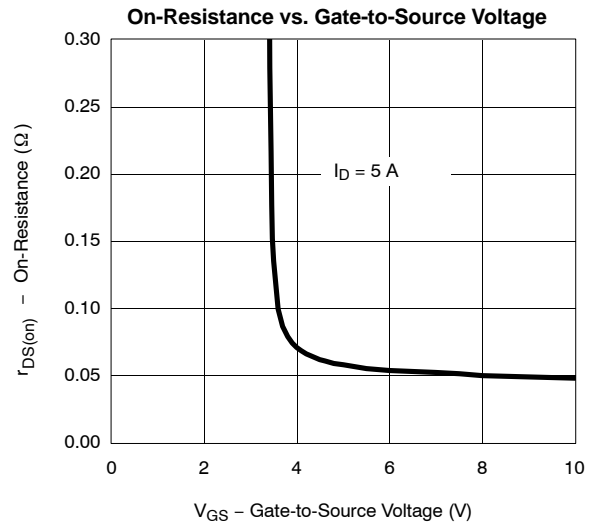
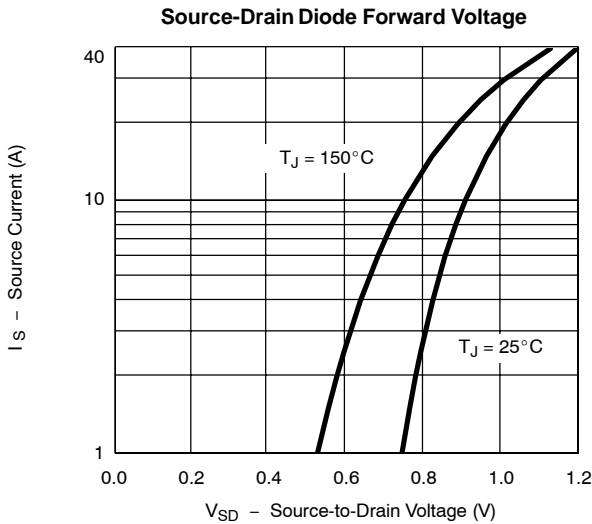
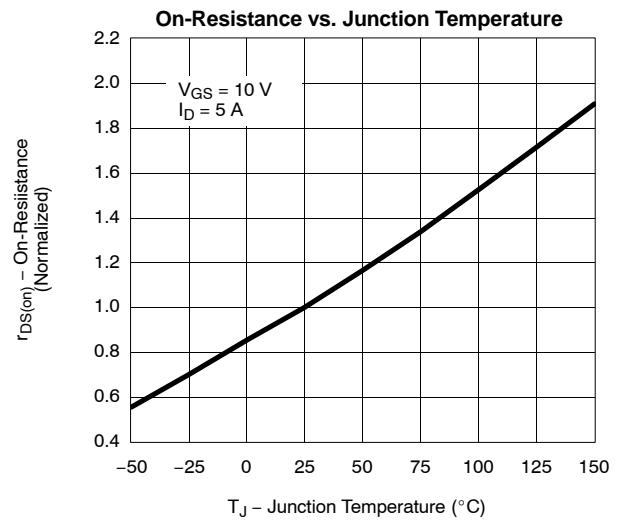
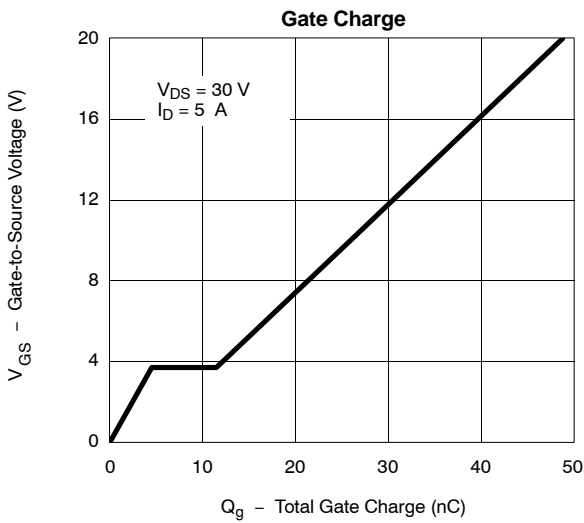
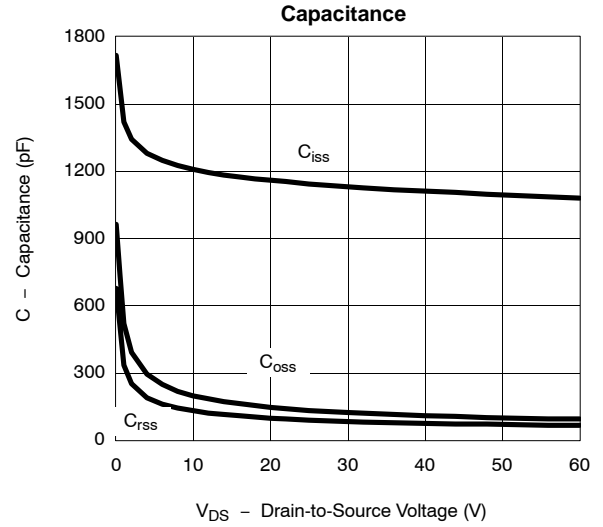
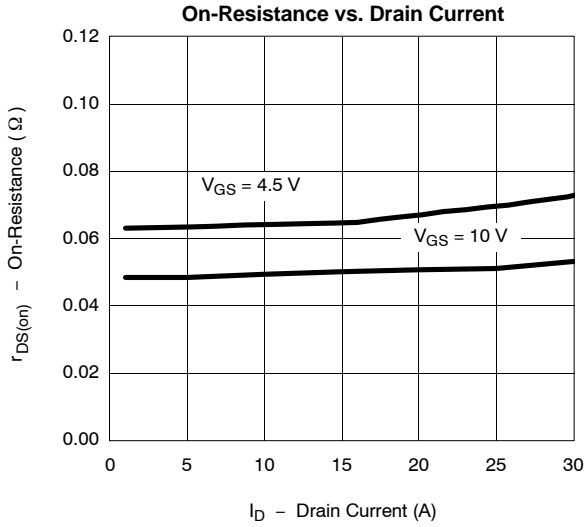
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

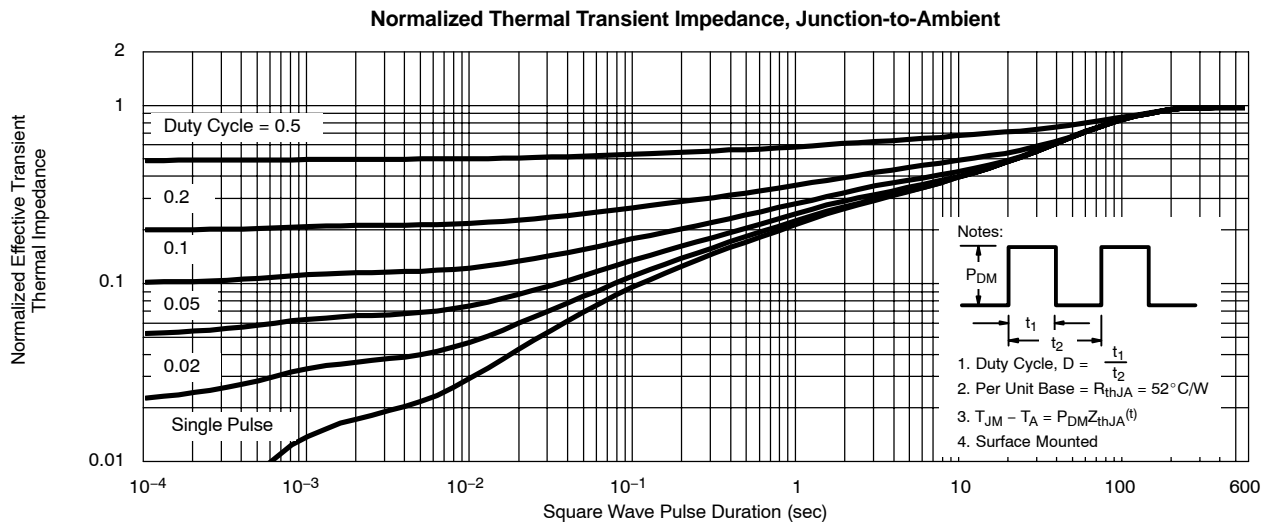
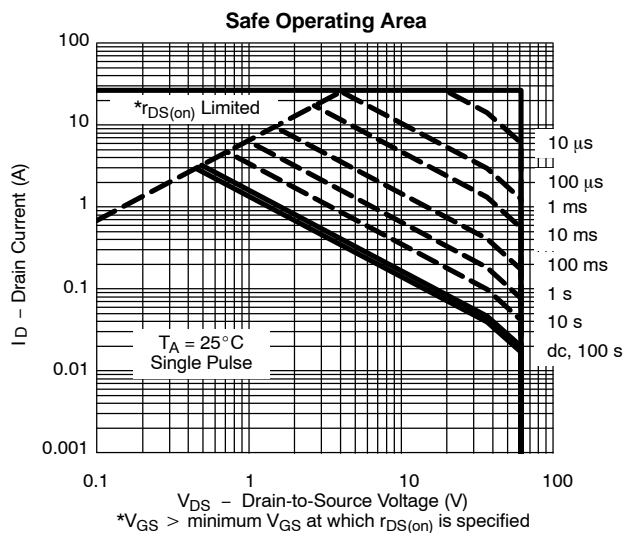
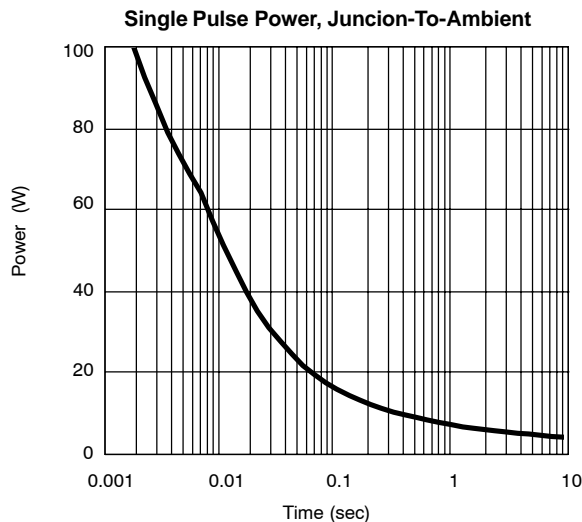
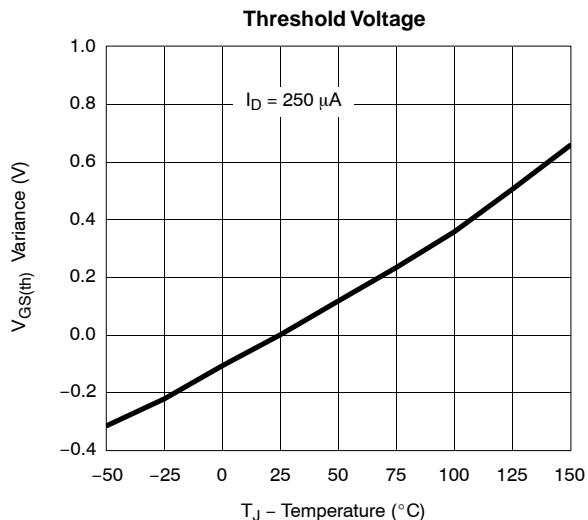
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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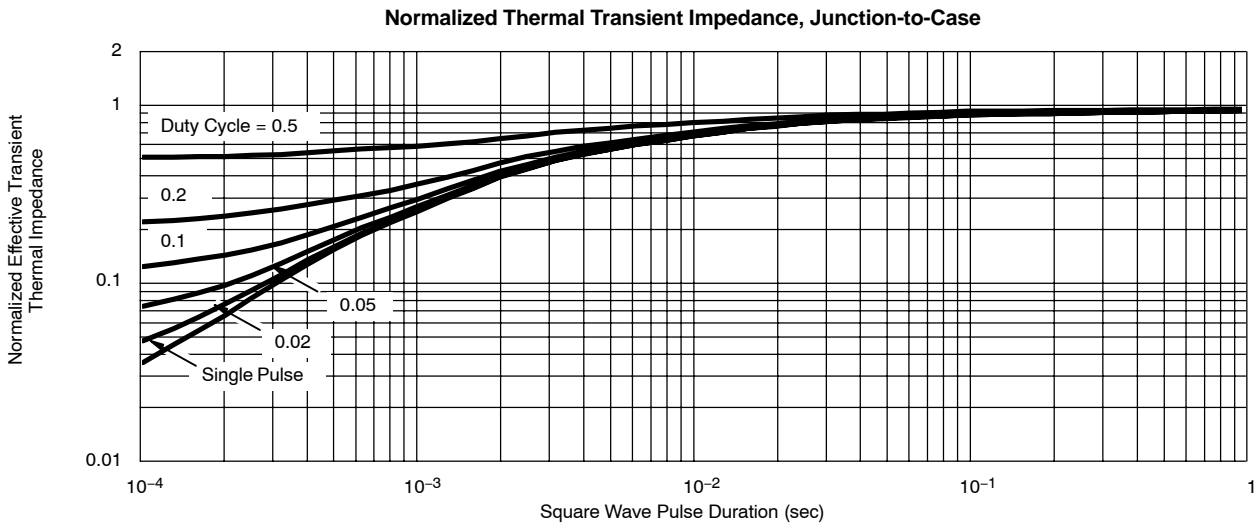


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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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